In the specification:

Please amend paragraph 24 as follows:

[24] With the detection and configuration circuit ***200***, the bidirectional buffer ***202*** may be programmed to operate in the desired direction without routing separate configuration lines to the memory elements ***212***, ***214*** associated with the buffer. Instead, the configuration signal is merely applied on one of the nodes ***204***, ***206*** that functions as the input and output nodes of the bidirectional buffer ***202***. The elimination of the separate configuration lines saves space in the integrated circuit containing the bidirectional buffers ***202***, allowing for the formation of additional functional circuitry in the integrated circuit such as additional bidirectional buffers are additional logic circuitry. Furthermore, elimination of the configuration lines simplifies the interconnection of components in the integrated circuit and thereby lowers the cost and improves the reliability of the integrated circuit, as will be appreciated by those skilled in the art.

Please amend paragraph 30 as follows:

[30] In the edge-triggered embodiment of **FIG. 3**, the flip-flop ***302***, ***304*** that is being disabled must not be clocked before the low input signal ***AL*** or ***AR*** has been applied to the input of that flip-flop, as will be appreciated by those skilled in the art. For example, if the configuration signal ***310*** is applied on node ***204*** then the ***BL*** signal output from flip-flop ***302*** must go high and then propagate through the inverter ***306*** to drive the ***AR*** signal low before the flip-flop ***304*** is clocked. If the ***AR*** signal is not low before the flip-flop ***304*** is clocked, then the ***BR*** signal will be latched high and enable the buffer circuit ***218***. In this situation, both buffer circuits ***216***, ***218*** would undesirably be enabled. The delay through the enabled buffer circuit ***216*** may be longer than the delay through the inverter ***306*** and thus there will be no problem with the flip-flop ***304*** being clocked before the ***AR*** signal goes low. Alternatively, one of the flip-flips ***302***, ***304*** could be positive edge triggered and the other negative edge triggered and this would eliminate any concern with the flip-flop being disabled (*i.e.*, flip-flop ***304*** in the present example) being clocked too quickly. The same potential

issue applies to clocking the flip-flop ***302*** when the configuration signal ***310*** is applied to node ***206*** to configure the buffer ***202*** to operate in the opposite direction, and the solutions just discussed with reference to flip-flop ***304*** apply to flip-flop ***302*** in this situation.